Module Description

GKWE 705 181 E, edition 03/89

ASEA BROWN BOVERI

PROCONTROL 44
Transfer

Telegram Handling Module

88 VT01-E/R1000

Application

The telegram handling module is used within a PROCONTROL master station.

Together with the modules 88 VA01/VA02 (control module for transfer procedure) and 88 VP01/VP02 (master station processor module) it forms part of the central processor within the master station. This processor controls and monitors the entire data transfer on the connected PROCONTROL remote bus system.

Features

The module can be plugged into each of the two master stations of the PROCONTROL bus system, but is only available once per station. It is provided with two standard interfaces: one of these is used to link the module to the master station bus to which all modules of the master station (including master station coupling modules 88 VK01) are connected. The second one is for the general bus which only connects the modules 88 VA01/VA02, 88 VP01/VP02 and 88 VT01/VT02 with each other.

Two light-emitting diodes and a test plug are provided at the front of the module.

Both light-emitting diodes serve to indicate disturbances that have been detected (see "Annunciation functions").

At the test plug, the most important transfer signals can be measured using an oscilloscope (see "Test functions").

Description

The telegram handling module is part of the entire master station bus control (consisting of modules 88 VA01/VA02, 88 VP01/VP02, 88 VT01/VT02). As an "auxiliary module" of the processor, it handles the serial telegrams.

However, each subfunction is only performed when called by a specific command from the processor module 88 VP01/VP02. The commands come from the command fields of the 48-bit data word of the program memory (see module description "Master station processor module 88 VP01/VP02", GKWE 705180). The commands are transferred in coded form via the general-bus and are decoded on the module (the decoders are not shown in the functional diagram).

In the following, the most important functional sections are specified and their functions within the entire program of the master station bus control are described (see also "Functional diagram").

SHIFT REGISTER

The central component of the module is a shift register, consisting of eight series-connected registers of 8 bits each.

Every response telegram arriving over the remote bus after a request by a multipurpose processing station, is passed on to this shift register. This takes place concurrently with the actual telegram distribution process whereby the telegrams are sent by the receiving coupling module 88 VK01 directly to all other coupling modules via the master station bus. Each telegram is immediately transferred from the shift register to the telegram memory in order to clear the shift register for the next telegram (see "Telegram memory"). This procedure is repeated for every telegram received.

If one or more stations signal an acknowledgement error to the master station during transfer of a telegram block, the processor prompts a repetition of the bring telegrams of this block (see module description "Master station processor module 88 VP01/VP02"). In this case, the telegrams are re-loaded from the telegram memory into the shift register and distributed again to the remote bus lines via the transfer logic and the master station bus.

If the master station transmits self-generated telegrams (e.g. call telegrams), these are compiled in the shift register and simultaneously loaded into the telegram memory for possible repetitions. To this end, the processor fetches the individual telegram sections (address, data, etc.), partly as constant, from its program (on 88 VP01/VP02), and also from the 88 VA01/VA02 (e.g. station address) or from the constant memory of the 88 VT01/VT02 (e.g. system address). During telegram generation, the shift register blocks for the check characters (CRC) are not loaded. The check characters (CRC) are generated by the appropriate circuit section during telegram transfer to the master station bus, and added to the current telegram as 15-bit CRC code (see "CRC logic").

Note: The start and end synchronizing signals by which a data telegram is extended on the remote bus, are separated (reception mode) or added (transmission mode) by the local bus coupling module 88 FN01/FN02. This applies to the master station as well as the multi-purpose processing station.

CRC LOGIC (CYCLIC REDUNDANCY CHECK)

Every telegram contains a field with 15 check characters. These are check bits, determined by means of a special generator polynominal, which secure the entire data contents of a telegram (function code, address, data) with the hamming distance d = 6 (CRC protection).

Every telegram received is checked for CRC errors. In this case, the CRC logic works as a test unit. If a CRC error is detected during telegram transfer (which means that one or more bits have been falsified), this is transferred, together with the telegram for identification purposes, to the telegram memory.

This error is also indicated on the module (see "Annunciation functions") and is signalled via the general-bus to the processor module which initiates a call repetition to ensure that error-free response telegrams are received.

If one of the receiving multi-purpose processing stations fails to acknowledge correct reception of a telegram during a telegram distribution process, the processor repeats the correctly received bring telegram stored in the telegram memory. While the distribution process is repeated, the CRC logic is switched to "Test". If a CRC error occurs between storage and selection of the telegram, module 88 VT01/VT02 is disturbed. This is also indicated on the module and communicated to the processor via the general-bus. This disturbance is simultaneously signalled via module output SST (common disturbance) to the master station bus (see "Annunciation functions").

Whenever the processor itself generates telegrams (e.g. call telegrams), the CRC logic works as a generator. For every telegram compiled in the shift register, the correct check bit combination is generated as required for the data contents, and added during the transfer process behind the data field in the security field.

BIT COUNTER

The bit counter serves to count the 63 clock pulses of the serial telegram.

The bit counter is used during transmission, reception and distribution of telegrams. It recognizes the 48th bit (last information bit) and the 63rd bit (last CRC bit) of a telegram. This information is further processed by the transmission and reception logic.

TRANSMISSION/RECEPTION LOGIC

These circuit sections mainly receive or generate the following three signals:

- Telegram data $\overline{TD}$ (real serial data telegram)
- Telegram clock $\overline{TT}$
- Telegram frame $\overline{TR}$

Telegram clock and telegram frame are special signals which are used to synchronize the modules of the master station during transfer of the data telegram.

The telegram clock for transmission is derived from a central clock frequency (input XCCLK, F = 1 MHz) which the module receives from the clock generator of processor module 88 VP01/VP02 via the master station bus.

TRANSMISSION ON GENERAL-BUS

Via the test signal and general-bus drivers, status signals of the module are transferred to the processor for further evaluation.

RECEPTION FROM THE GENERAL-BUS

Conversely, all data transferred by other modules (88 VP01/VP02, 88 VA01/VA02) to the telegram handling module via the general-bus are switched by the second general-bus driver to the module-internal 8-bit bus.

CONSTANT MEMORY

This memory has to be programmed user-oriented and contains a number of items of information which are needed by the processor, among other things, for compiling master station telegrams (see "Programming note").

To read the individual memory locations, the processor writes the corresponding address into the constant memory address registers. By corresponding control commands, the respective memory location content is then switched to the module-internal 8-bit bus.

TELEGRAM MEMORY

This memory serves to buffer 8 telegrams for telegram repetition after transfer errors.

The telegrams are buffered so that they can be distributed again if acknowledgement errors are signalled from one (or more) multi-purpose processing station(s). This, however, only applies to bring telegrams.

Moreover, request telegrams transferred by a multi-purpose processing station are converted into another code in the function code field before they are transferred further. They are not transferred if a distribution process is repeated. Using request telegrams, every bus-connected module can request data from every other bus-connected module.

Every incoming telegram is checked for CRC errors, (see "CRC logic"). If a CRC error is detected, a CRC error bit, in addition to the telegram, is transferred to the telegram memory.

In the telegram memory, as in the constant memory, every memory location to which a telegram is to be written must be selected by an address. For this, a telegram memory address register and an address multiplexer are available.

Shift register block and memory location of the telegram memory have a word width of 8 bits. Therefore, eight memory locations of the telegram memory are required for a complete telegram (function code up to CRC 0-byte). The individual eight memory location addresses can be selected by the processor via the multiplexer within this range (= telegram byte addressing). The address of the first memory location needed for a telegram is written by the processor into the telegram memory address register (= telegram addressing).

Test functions

The front of the module is provided with a test plug X1 at which the following signals can be measured (Fig. 1 shows the contact positions):

K1: TD = data telegram } for transmission,
K2: TT = telegram clock } reception,
K3: TR = telegram frame } distribution
K4: Intern. signal "transmission", synchr. with TR
K5: Intern. signal "distribution", synchr. with TR
K6: CRC error
K7: Central clock pulse P30 (F = 2.5 MHz)
K8: not used
K9: ZD = reference potential

Signals K1 - K7 may only be measured via a high resistance.

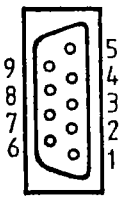


Figure 1

Note:
Valid oscilloscope displays can only be obtained by means of a logic analyzer which generates a trigger signal for the oscilloscope. The logic analyzer has to be connected to the module test plug of the 88 VP01/VP02 module. The same applies to the master station coupling module 88 VK01.

Annunciation functions

ANNUNCIATION FUNCTIONS ON THE MODULE

Two light-emitting diodes are provided at the front of the modules.

The red light-emitting diode STV (= Disturbance Distribution) emits a light signal when an error-free, buffered received telegram suddenly contains a CRC error (= module disturbance) when being further transferred.

The red light-emitting diode STE (= Disturbance Reception) emits a light signal when a CRC error has been detected in a received telegram. In addition, the CRC error pulse is extended to approx. 100 ms via a monostable timing element.

ANNUNCIATION FUNCTIONS TO THE MASTER STATION BUS

A detected CRC error (light-emitting diode STV) which results from a module disturbance is switched via output SST (common disturbance) to the master station bus. This signal is evaluated by the coupling module for monitoring station 88 VU01 (see module description "Coupling module for monitoring station 88 VU01", GKWE 705 190).

The annunciation STV is stored in the module and can only be reset by a program command (at the beginning of a system cycle).

Programming note

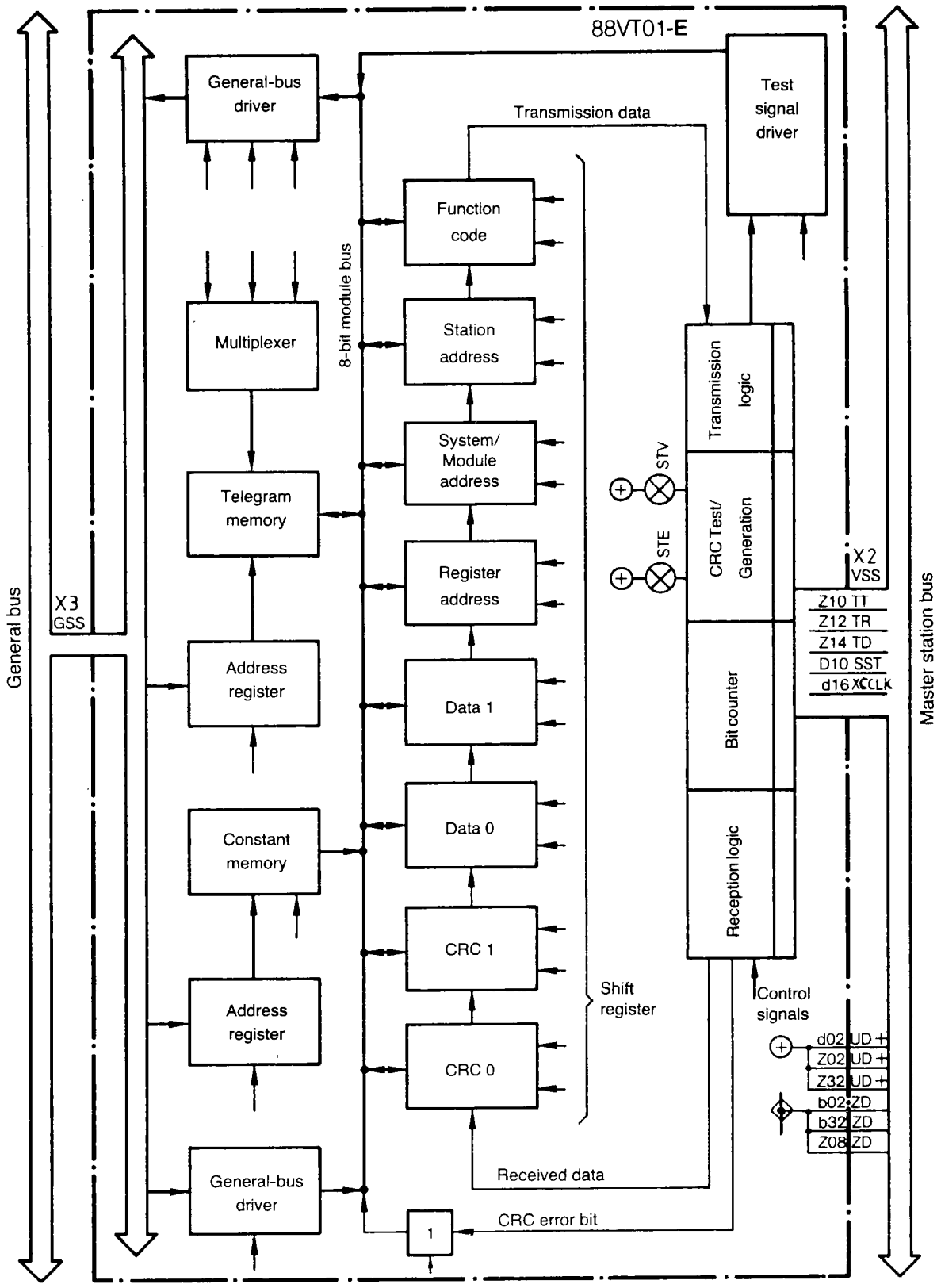
The constant memory (A209) has to be programmed user-oriented. The memories for use in master stations A and B differ with respect to their content. The following list shows the content, where "X" represents user-related information.

Address:	Content VSA: MSB	LSB	Content VSB: MSB	LSB	Explanation:
000 to 0FF	Free		Free		
100	xx11	1111	xx11	1111	System/Common module address 63
101	xx11	1100	xx11	1101	System/Common address (60/61 = 88 TK02)
102	1111	1101	1111	1110	Master station address (A = 253, B = 254)
103	0000	xxxx	0000	xxxx	Highest available PDDS address (1 ≤ PDDS address ≤ 8)
104	1111	1011	1111	1011	Short request criteria (= 251)
105	1111	0111	1111	0111	Short request criteria with continuous noise generating module (= 247)
106	xx11	1110	xx11	1110	System/Module address (88 TV01 = 62)
107	1010	1010	1010	1010	Start Cycle identification (Test: Module/PROM available)
108	0000	xxxx	0000	xxxx	Highest available remote bus line number
109	0010	0000	0010	0000	Max. number of event telegrams per event processing (= 32)
10A	0001	1000	0001	1000	Max. number of event telegrams per event processing for continuous noise generating module (= 24)
10B	1110	1101	1110	1101	Setting of call counter to identify a continuous noise generating module (= 237)
10C	1111	1100	1111	1100	Setting of counter for 2nd repetition call to identify a continuous noise generating module (= 252)
10D	1111	111x	1111	111x	x = 0 when using optical waveguides up to 5 km length x = 1 in all other cases
10E to 1FE	Free		Free		
1FF or	0101	0101	-	-	Non-redundant mode (only VSA)
1FF	1111	1111	1111	1111	Redundant mode (VSA and VSB)

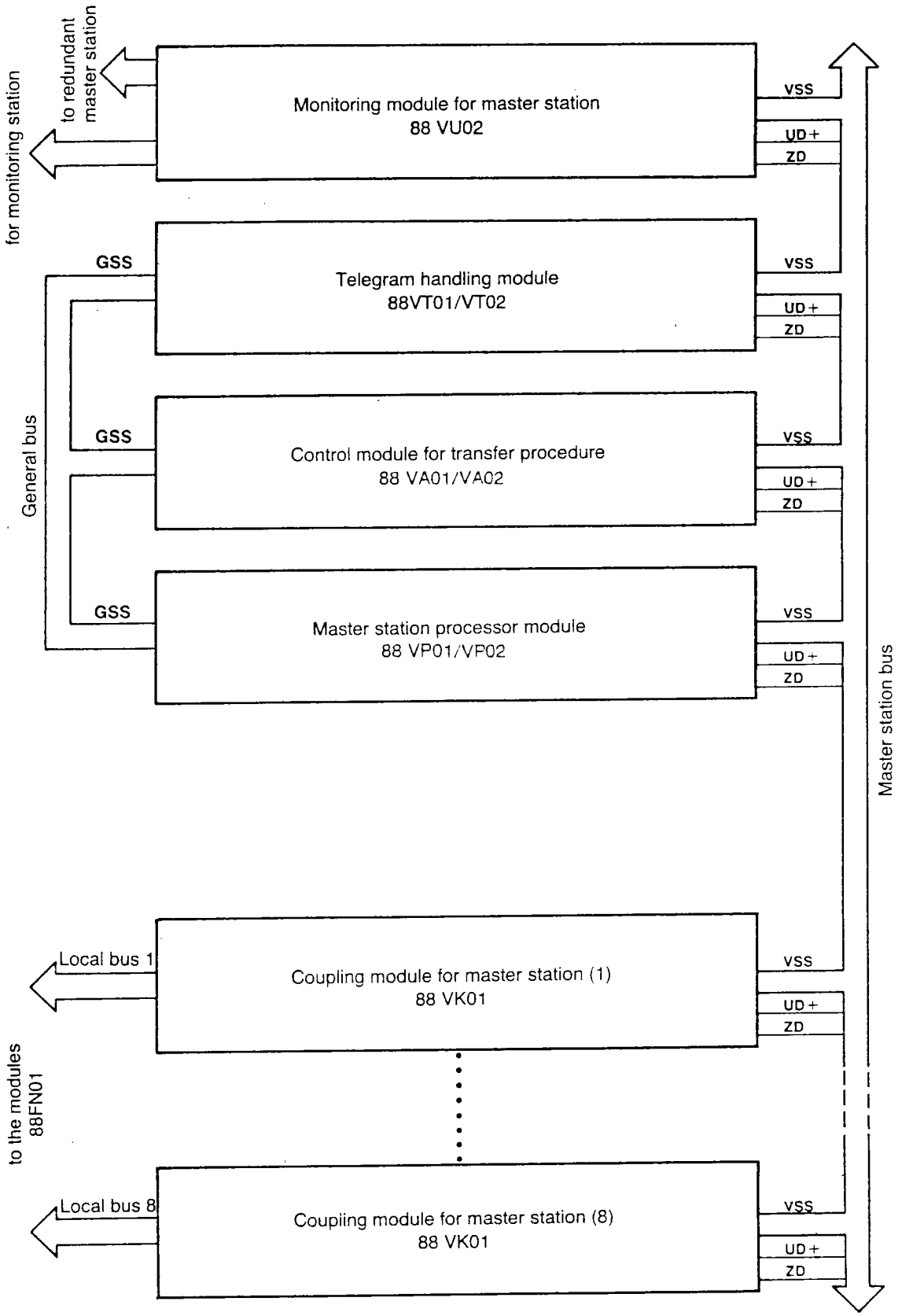
Functional diagram

The module is equipped with connectors X2 and X3 (see "Mechanical design"). Connector X2 incorporates the interface to the master station bus and the voltage supply.

Connector X3 incorporates the interface to the general-bus.



Connection diagram in the master station



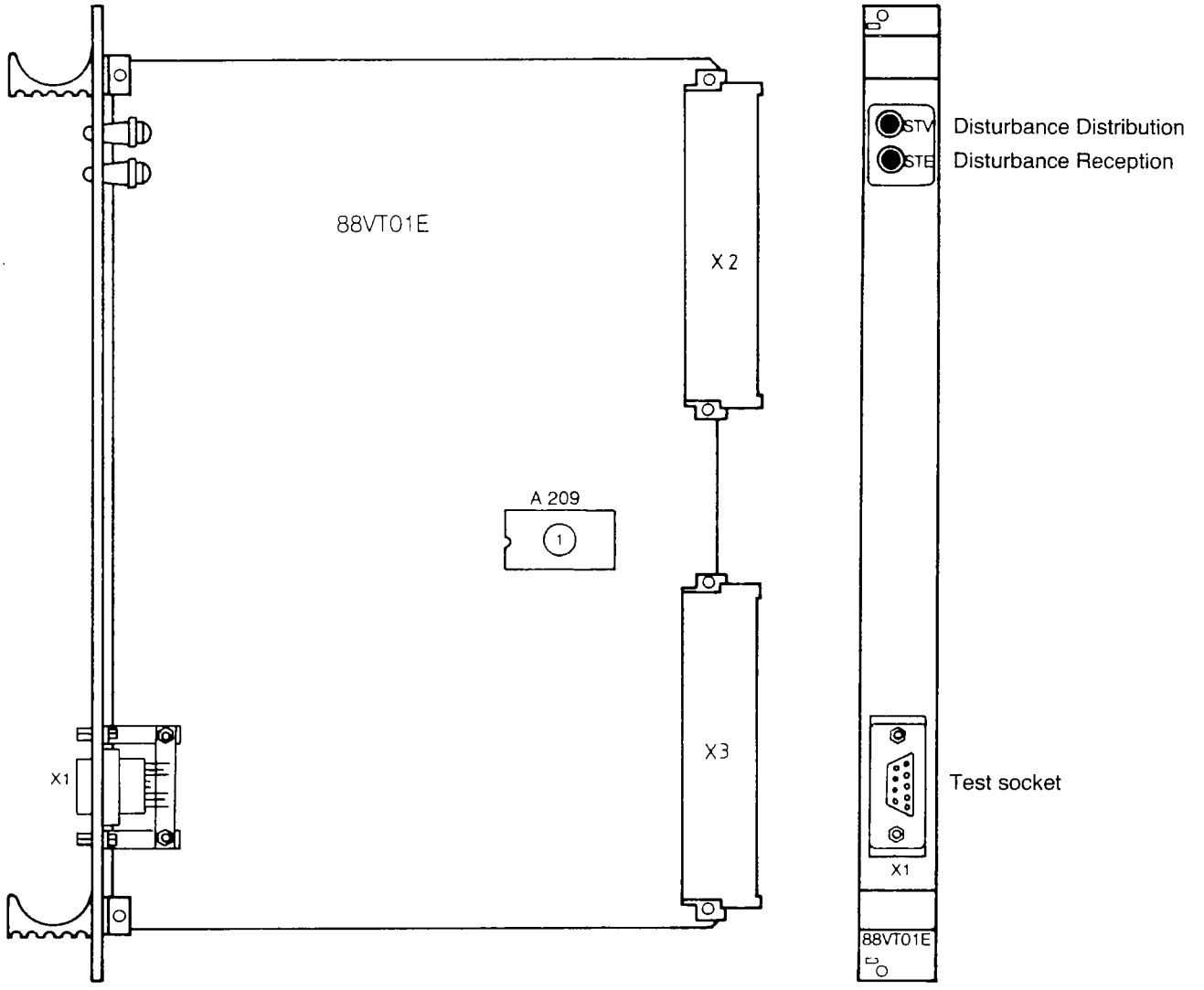
Mechanical design

Board size: 6 units, 1 division, 220 mm deep

Connector: according to DIN 41 612
2 x 48-pole, edge connector type F (for X2 and X3)
to MIL C-24 308
1 x 9-pole, female connector type HD (for X1)
(Fabricated by AMP)

Weight: approx. 0.4 kg

POSITION OF MEMORY MODULE ON THE PRINTED CIRCUIT BOARD AND FRONT PANEL



Memory module:

① = Constant memory

Order number:
(component)
GJTN160053P1

Important:
The module should only be plugged into the slot range 09 - 45 (general-bus range, lower connector) of the master station (double subrack AA, AB).

Technical data

In addition to the system data the following values apply:

POWER SUPPLY

Operating voltage	UD+ = +5 V
Current consumption	I_D = 1.2 A
Power dissipation typ.	P_V = 6 W
Reference potential	ZD = 0 V

STANDARD CONNECTIONS

VSS - standard interface to master station bus
$\overline{TT}$ - telegram clock *
$\overline{TR}$ - telegram frame *
$\overline{TD}$ - telegram data (serial data telegram) *
$\overline{SST}$ - common disturbance *
XCCLK - central clock frequency (1 MHz)
GSS - standard interface to general bus

* These signals are transmitted inversely.

ORDERING DATA

Type designation: 88 VT01-E/R1000 **

Order number: GJR2313000R1000 **

** 88 VT01-E/R1000 is to be replaced by
88 VT02-E/R1000

Technical data are subject to change without notice!

ABB Kraftwerksleittechnik GmbH

P. O. Box 100351, D–68128 Mannheim
Phone (0621) 381 2712, Telefax (0621) 381 4372
Telex 462 411 107 ab d

Printed in Germany (PPC/R11 0898 BSV)